AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1. (currently amended) An address translation filter for filtering a signal on a system bus that couples between a core processor and an external memory unit, the address translation filter comprising:

a first interface operable under a first bus protocol to connect to the system bus and receive a virtual memory address from an external device connected to the bus;

a second interface operable under a second bus protocol to connect to the system bus and transmit a physical memory address to the external memory unit;

an input for receiving an input system clock signal;

an output for transmitting an output system clock signal; and

an address translation unit, comprising a translation lookaside buffer and a refresh logic unit operable to refresh the translation lookaside buffer if the virtual memory address is not matched by an entry in the translation lookaside buffer, the address translation unit being external to the core processor and coupled between the first and second

interfaces, operable to determine the physical memory address from the virtual memory address,

wherein the first bus protocol is the same as the second bus protocol, and wherein the output clock signal is paused while the translation lookaside buffer is being refreshed.

2. (original) An address translation filter in accordance with claim 1, wherein the address translation unit includes a lookup table indexed by virtual addresses.

3. (original) An address translation filter in accordance with claim 2, wherein the lookup table is indexed by the most significant portion of a virtual address.

4. (canceled)

5. (canceled)

6. (previously presented) An address translation filter in accordance with claim 5, further comprising:

an output control link responsive to the refresh logic unit and operable to signal the core processor when the translation lookaside buffer is to be refreshed.

7. (canceled)

8. (original) An address translation filter in accordance with claim 1, wherein the virtual and physical memory addresses have the same width.

9. (currently amended) ~~An integrated circuit~~A digital processing system, comprising:

a core processor;

a processing device external to the core processor;

an address translation filter comprising a translation lookaside buffer having an input for receiving an input system clock signal and an output for transmitting an output system clock signal; and

a system bus operable to link the core processor and the address translation filter to each other under a bus protocol and to link the processing device to the address translation filter under the same bus protocol,

wherein the address translation filter [[unit]] is operable to translate a virtual memory address received via the system bus from the processing device into a physical memory address in an external memory unit and to transmit the physical memory address to the external memory unit via the system bus, and wherein the output clock signal is paused while the translation lookaside buffer is being refreshed.

10. (currently amended) ~~An integrated circuit~~A digital processing system in accordance with claim 9, wherein the address translation filter further comprises:

~~a translation lookaside buffer; and~~

a refresh logic unit operable to refresh the translation lookaside buffer when the virtual memory address is not matched by an entry in the translation lookaside buffer.

11. (currently amended) ~~An integrated circuit~~A digital processing system in accordance with claim 10, wherein the address translation filter further comprises:

an output control link responsive to the refresh logic unit and operable to send a refresh signal the core processor when the translation lookaside buffer is to be refreshed.

12. (currently amended) ~~An integrated circuit~~A digital processing system in accordance with claim 10, wherein the core processor is operable to refresh the translation lookaside buffer when a refresh signal is received from the address translation filter.

13. (currently amended) ~~An integrated circuit~~A digital processing system in accordance with claim 12, wherein the translation lookaside buffer is refreshed via the system bus.

14. (currently amended) A digital processing system comprising:

a core processor;

an external memory unit;

an external processing device;

an address translation filter comprising a table of physical memory addresses indexed by virtual address, an input for receiving, an input system clock signal and an output for transmitting an output system clock signal; and

a system bus linking the core processor, the external memory and the address translation filter to each other and linking the external processing device to the address translation filter,

wherein the address translation unit is operable to translate a virtual memory address received via the system bus from the external processing device into a physical memory address transmitted via the system bus to the external memory unit [[and]], wherein the bus is one of an AMBA bus and an AHB bus and wherein the output clock signal is paused while the table of physical memory addresses is being refreshed.

15. (currently amended) A method of memory address translation in ~~an integrated circuit~~ a bus coupled between a core processor ~~in the integrated circuit~~ and an external memory unit, the method comprising:

receiving a first bus signal from a device ~~in the integrated circuit~~ via the bus in accordance with a first bus protocol;

translating a virtual memory address specified by the first bus signal to a physical memory address by selecting a physical memory address from a table of physical memory addresses indexed by virtual

addresses;~~in an address translation filter in the integrated circuit; and;~~

refreshing the table of physical memory addresses if the table has no entry for the virtual address;

transmitting a second bus signal via the bus to the external memory unit in accordance with a second bus protocol, the second bus signal specifying the physical memory address;

transmitting a system clock signal; and

pausing the system clock signal while the table of physical memory addresses is being refreshed.

~~wherein the first bus protocol is the same as the second bus protocol.~~

16. (canceled)

17. (canceled)

18. (currently amended) A method in accordance with claim 15[[17]], wherein the refreshing comprises receiving data via the bus from the core processor coupled to the bus.

19. (currently amended) A method in accordance with claim 15[[17]], wherein the refreshing comprises:

signaling the core processor that the table of physical memory addresses needs to refreshed;

passing the virtual memory address to the core processor; and

receiving a new physical memory address from the core processor.

20. (currently amended) A method ~~in accordance with claim 15~~ of memory address translation in a bus coupled between a core processor and an external memory unit, the method comprising:

receiving a first bus signal from a processing device via the bus in accordance with a first bus protocol;

translating a virtual memory address specified by the first bus signal to a physical memory address in an address translation filter by selecting a physical memory address from a table of physical memory addresses, the table of physical memory addresses being indexed by virtual addresses;

refreshing the table of physical memory addresses if the table has no entry for the virtual address; and

transmitting a second bus signal via the bus to the external memory

unit in accordance with a second bus protocol, the second bus signal specifying the physical memory address,

~~wherein the first bus signal is received from a processing device, further comprising:~~

providing a system clock signal to the processing device; and

pausing the system clock signal while the table of physical memory addresses is being refreshed;

wherein the first bus protocol is the same as the second bus protocol.

21. (previously presented) A method in accordance with claim 15, wherein the second bus signal is transmitted to the external memory unit.

22. (original) A method in accordance with claim 15, wherein the first bus signal is received from a processing device.

23. (currently amended) A method ~~in accordance with claim 22, further comprising:~~ of memory address translation in a bus coupled between a core processor and an external memory unit, the method comprising:

receiving a first bus signal from a processing device via the bus in accordance with a first bus protocol;

translating a virtual memory address specified by the first bus signal to a physical memory address in an address translation filter by selecting a physical memory address from a table of physical memory addresses, the table of physical memory addresses being indexed by virtual addresses;

refreshing the table of physical memory addresses if the table has no entry for the virtual address;

transmitting a second bus signal via the bus to the external memory unit in accordance with a second bus protocol, the second bus signal specifying the physical memory address,

transferring code from a core processor to the processing device; and

transferring an initial memory map from the core processor to the address translation filter.

24. (previously presented) A digital processing system in accordance with claim 9, wherein the bus is one of an AMBA bus and an AHB bus.

25. (currently amended) A digital processing system in accordance with claim 14, wherein the table of physical memory addresses comprises a translation lookaside buffer and wherein the address translation filter further comprises:

~~a translation lookaside buffer; and~~

a refresh logic unit operable to refresh the translation lookaside buffer [[when]] if the virtual memory address is not matched by an entry in the translation lookaside buffer.

26. (previously presented) A digital processing system in accordance with claim 25, wherein the address translation filter further comprises:

an output control link responsive to the refresh logic unit and operable to send a refresh signal the core processor when the translation lookaside buffer is to be refreshed.

27. (previously presented) A digital processing system in accordance with claim 26, wherein the core processor is operable to refresh the translation lookaside buffer when a refresh signal is received from the address translation filter.

28. (previously presented) A digital processing system in accordance with claim 27, wherein the translation lookaside buffer is refreshed via the system bus.

29. (currently amended) A digital processing circuit, comprising:

a core processor;

a processing device external to the core processor;

a system bus coupled to the core processor and operable to link the core processor to an external memory unit under a system bus protocol;

an address translation filter comprising a table of physical addresses indexed by virtual addresses, the address translation filter being operable to couple the processing device to the system bus under the same system bus protocol,

wherein the address translation [[unit]] filter is operable to translate a virtual memory address received via the system bus from the processing device into a physical memory address, in the external memory, transmitted via the system bus to the external memory unit and is further operable to pause a system clock supplied to the processing device if the table of physical memory addresses has no entry for a virtual address received from the processing device.

30. (currently amended) A digital processing circuit in accordance with claim 29, wherein the system bus comprises an ~~core processor, the address translation filter and the processing device occupy the same integrated circuit system~~ Advanced High-performance Bus.

31. (previously presented) A digital processing system in accordance with claim 29, wherein the system bus has an Advanced Micro-controller Bus Architecture.